ABSTRACT OF THE DISCLOSURE

A memory cell includes first and second p-channel transistors and first and second n-channel transistors in a cross-coupled latch configuration. Power control circuitry associated with the memory cell is coupled to selectively perform voltage transitions on the source terminals of one or more of the n-channel and/or p-channel transistors in the memory cell during a data corruption mode of operation to destroy data stored in the latch and set the memory cell to a known state. In one implementation, the power control circuitry is coupled to the source terminal of one of the n-channel transistors to transition that terminal from a low voltage reference level (present during a normal mode of operation) to a high voltage reference level and back to the low voltage reference level. In another implementation, the power control circuitry is coupled to the source terminal of one of the n-channel transistors and the source terminal of at least one of the p-channel transistors. The power control circuitry a) transitions the p-channel source terminal from a high voltage reference level (present during a normal mode of operation) to a low voltage reference level and back to the high voltage reference level, and b) transitions the n-channel source terminal from a low voltage reference level (present during a normal mode of operation) to a high voltage reference level and back to the low voltage reference level.